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Description

[SLEW RATE ENHANCEMENT CIRCUIT VIA DYNAMIC OUTPUT STAGE]

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 92105571, filed March 14, 2003.

BACKGROUND OF INVENTION

[0002] Field of Invention

[0003] The present invention relates to a slew rate enhancement circuit. More particularly, the present invention relates to a slew rate enhancement circuit which is compact and occupies small chip area.

[0004] Description of Related Art

[0005] To achieve high slew rate, when the operational amplifier ("OPAMP") drives heavy load. Many techniques are used to enhance slew rate, such as: increase operating current of OPAMP, reduce compensation capacitor, or connect with error amplifier. Except for the high slew rate, a lot of dis-

advantages such as high operating current and stability degradation for original OPAMP, a large chip area, complexity of circuit design, noise and offset are introduced from error amplifiers succeed.

[0006] FIG. 1 illustrates a high slew rate amplifier according to a prior art. The circuit in FIG. 1 includes an OPAMP 102, error amplifiers 104, 106 and a push-pull output stage 112. The push-pull output stage includes a P-type Metal Oxide Semiconductor ("PMOS") transistor 108 and a N-type Metal Oxide Semiconductor ("NMOS") transistor 110. The inverting inputs of the error amplifier 104 and the error amplifier 106 are connected with the output of the OPAMP 102 at a node N11. The non-inverting inputs of the error amplifier 104 and the error amplifier 106 are connected with a load at a node N12. The loop of connection between the output of the error amplifier 104 and the gate of the PMOS transistor 108, and the loop of connection between the drain of the PMOS transistor 108 and the inverting input of the error amplifier 104 formed a negative feedback loop. Likewise, the loop of connection between the output of the error amplifier 106 and the gate of the NMOS transistor 110, and the loop of connection between the drain of the NMOS transistor 110 and the inverting in-

put of the error amplifier 106 also formed a negative feedback loop. The node N11 and the loop including node N12 construct a virtual short loop. The virtual short loop and both of the negative feedback loops are applied for controlling the PMOS transistor 108 to push current to the load or the NMOS transistor 110 to pull current from the load.

[0007] The error amplifier 104 and the error amplifier 106 are applied for monitoring the output signals of the OPAMP 102. When a non-inverting input Vin10 is not equal to an inverting input Vout10, the error amplifier 104 and the error amplifier 106 will turn on the PMOS transistor 108 to push a current to the load, or turn on the NMOS transistor 110 to pull a current from the load. On the other hand, when the signal Vin10 is equal to the signal Vout10, the PMOS transistor 108 and the NMOS transistor 110 will work under the DC bias condition.

[0008] In general, the circuit of FIG. 1 is usually applied for buffer amplifier. In order to provide a large current from the PMOS transistor 108 and the NMOS transistor 110, the aspect ratios of the PMOS transistor 108 and the NMOS transistor 110 should be as large as possible, but the static operating current will also be increased according to

the aspect ratio. Furthermore, the real circuit on a chip is more complicated than FIG. 1 appears, since the error amplifier 104 is constructed by at least 5 pieces of Metal Oxide Semiconductor ("MOS") transistors, and so is the error amplifier 106. If the Miller Compensation is applied for compensating the pole/zero location shifts, another two compensation capacitors are introduced into the circuit of FIG. 1. If the offset voltage, symmetry of layout, cross distortion, linearity, bandwidth and noise of and from the error amplifier 104 and error amplifier 106 are calibrated, additional circuits will be added to the circuit of FIG. 1. Therefore, the manufacturing of the circuit of FIG. 1 on a chip will occupy a huge chip area and consume high static operating current for the original OPAMP.

SUMMARY OF INVENTION

[0009] As embodied and broadly described herein, the invention provides an improved circuit, denoted as the dynamic output stage for enhancement of the slew rate. The original operational amplifier includes a differential amplifier and a main output stage. The dynamic output stage includes a monitoring stage and an assistant output stage. The main output stage detects an input voltage from a differential amplifier to decide for outputting a main cur-

rent to the load or not. The main output stage also generates a push signal and a pull signal for the monitoring stage. The monitoring stage decays the push signal and the pull signal, and the assistant output stage will receive the decayed push signal and the decayed pull signal to decide for providing an assistant current to the load or not. The assistant current is an additional huge current for enhancing the slew rate. The assistant current is turned on/off automatically and will not affect the operation status of the original OPAMP and the main output stage. Furthermore, the dynamic output stage does not consume static operating current. Compare with the error amplifiers in the prior art, this invention will not introduce the offset voltage, compensation, distortion and noise Therefore, no calibration will be necessary.

[0010] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF DRAWINGS

[0011] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The

drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0012] Fig. 1 is a high slew rate amplifier according to a prior art.

[0013] Fig. 2 is a sketch of the dynamic output stage of a preferred embodiment of the present invention.

[0014] Fig. 3 is a detail circuit of the dynamic output stage of a preferred embodiment of the present invention.

[0015] Fig. 4 is the graph of the final push current and the final pull current at the node N25 versus the push and pull signal of OPAMP with and without this art.

DETAILED DESCRIPTION

[0016] FIG. 2 illustrates a sketch of the dynamic output stage of a preferred embodiment of the present invention. An OPAMP includes a differential amplifier 202 and a main output stage 204. The differential amplifier has an inverting input, denoted as Vout 20 and a non-inverting input, denoted as Vin 20. The output of differential amplifier, denoted as node N21, is connected with the main output stage 204. The main output stage 204 includes a plurality of sub-circuits: a voltage source 220, a PMOS transistor 216, a voltage source 222 and a NMOS transistor 218. The

output of the differential amplifier 202 is connected with the voltage source 220 and the voltage source 222 at a node N21. The drain of PMOS transistor 216 is connected with the drain of NMOS transistor 218 at a node N22. The gate of PMOS transistor 216 is connected with the voltage source 220 and with a voltage source 208 at a node N23. A push signal Vg1 is generated by the main output stage 204 at the node N23 and the signal Vg1 also denotes the voltage of the node N23. The source of the PMOS transistor 216 is connected with an input power Vdd. The gate of NMOS transistor 218 is connected with the voltage source 222 and with a voltage source 210 at a node N24. A pull signal Vg2 is generated by the main output stage 204 at the node N24 and the signal Vg2 also denotes the voltage of the node N24. The source of the NMOS transistor 218 is connected with ground. The voltage of the voltage source 208 is V1 and the voltage of the voltage source 210 is V2. An assistant output stage 206 includes a PMOS transistor 212 and a NMOS transistor 214. The drain of the PMOS transistor 212 is connected with the drain of the NMOS transistor 214 at a node N25. The node N22 is connected with the node N25 and the load. The gate of the PMOS transistor 212 is connected with the voltage source

208 and the gate of the NMOS transistor 214 is connected with the voltage source 210.

[0017] In steady state, the voltage Vin20 is equal to the voltage Vout20, the main output stage 204 does not apply any current to the load. A decayed push signal Vg3, denoting the gate voltage of the PMOS transistor 212 is equal to the push signal Vg1 minus the voltage V1. The voltage V1 is large enough, so the decayed push signal Vg3 is not able to turn on the PMOS transistor 212. Likewise, a decayed pull signal Vg4, denoting the gate voltage of the NMOS transistor 214 is equal to the pull signal Vg2 minus the voltage V2. The voltage V2 is large enough, so the decayed pull signal Vg4 is not able to turn on the NMOS transistor 214. No current will be applied to the load from the assistant output stage 206.

[0018] When the steady state no longer exists, the voltage Vin20 is much larger than the voltage Vout20. The output node N21 of differential amplifier 202 will approach to gnd. The gate voltage N23 of PMOS 216 will approach to gnd, too. Thus, the PMOS 216 will apply a main current to the load from node N22. The push signal Vg1 is fed forward to assistant output stage 206 via the voltage source 208. The push signal Vg1 is decayed by the voltage source 208,

wherein generated a decayed push signal Vg3. This result in decayed push signal Vg3 will approach to gnd, even though the potential voltage of Vg3 is "Vg1+V1". The decayed push signal is large enough to turn on the PMOS 216. Meanwhile, the gate voltage N24 of NMOS 218 will approach to gnd, thus the NMOS 218 is turned off. The pull signal Vg2 is fed forward to assistant output stage 206 via the voltage source 210. The pull signal Vg2 is decayed by the voltage source 210, wherein generated a decayed pull signal Vg4. This result in decayed pull signal will approach to gnd, and the NMOS 214 is turned off. Therefore, the assistant output stage 206 will also apply an assistant current to the load from the node N25. When the voltage Vin20 turns into a little larger than the voltage Vout20, the gate voltage N23 of PMOS 216 and the gate voltage N24 of NMOS 218 will return to steady state condition. Due to the voltage source 208 and 210, the assistant output stage 206 will turn off and no longer apply an assistant current to load. The main output stage will apply current to the load until the voltage Vin20 equals to Vout20.

[0019] When the voltage Vin20 is much smaller than the voltage Vout20, the output node N21 of differential amplifier 202

will approach to vdd. The gate voltage N24 of NMOS 218 will approach to Vdd, too. Thus, the NMOS 218 will apply a main current to load from node N22. The pull signal Vg2 is feed forward to assistant output stage 206 via the voltage source 210. The pull signal Vg2 is decayed by the voltage source 210, wherein generated a decayed push signal Vg4. This result in decayed pull signal Vg4 will approach to Vdd, even though the potential voltage of vg4 is "Vg2+V2". The decayed pull signal is large enough to turn on the NMOS 214. Meanwhile, the gate voltage N23 of PMOS 216 will approach to Vdd, thus the PMOS 216 is turned off. The push signal Vg1 is fed forward to assistant output stage 206 via the voltage source 208. The push signal Vg1 is decayed by the voltage source 208, wherein generated a decayed push signal Vg3. This result in decayed pull signal will approach to Vdd, and the PMOS 212 is turned off. Therefore, the assistant output stage will also apply an assistant current to the load from the node N25. When the voltage Vin20 turns into a little smaller than the voltage Vout20, the gate voltage N23 of PMOS 216 and the gate voltage N24 of NMOS 218 will return to steady state condition. Due to the voltage source 208 and 210, the assistant stage 206 will turned off and no longer

apply an assistant current to the load. The main output stage will apply current to the load until the voltage Vin20 equals to Vout20. The novel technology presented above is the dynamic output stage.

[0020] FIG. 3 is a detail circuit of the dynamic output stage in the present invention, wherein the voltage sources 208 and 210 are replaced by a monitoring stage 302. The monitoring stage 302 includes a PMOS transistor 304, a current source 308, a NMOS transistor 306 and a current source 310. The gate of the PMOS transistor 304 is connected with the gate of the PMOS transistor 216 at the node N23. The source of the PMOS transistor 304 is connected with the gate of the PMOS transistor 212 and with the current source 308 at a node N26. The drain of the PMOS transistor 304 is connected with ground. The gate of the NMOS transistor 306 is connected with the gate of the NMOS transistor 218 at the node N24. The source of the NMOS transistor 306 is connected with the gate of the NMOS transistor 214 and with the current source 310 at a node N27. The other circuit devices and connections in FIG. 3 are the same as those in FIG.2.

[0021] In FIG. 3, when the voltage Vin20 is equal to the voltage Vout20 in the steady state, the main output stage 204

does not apply any current to the load. The PMOS transistor 216 and the NMOS transistor 218 will work under quiescent current bias condition. The voltage difference between the node N26 and the node N23 will be equal to a threshold voltage Vt1 of PMOS 304 at least. Likewise, the voltage difference between the node N27 and the node N24 will be equal to a threshold voltage Vt2 of NMOS 306 at least. The push signal Vg1 is decreased by the threshold voltage Vt1, and therefore the decayed push signal Vg3 will equal to Vdd, thus the PMOS transistor 212 will be turned off. The pull signal Vg2 is also decreased by the threshold voltage Vt2, and therefore the decayed pull signal Vg4 will equal to ground, thus the PMOS transistor 212 will also be turned off. Therefore, the assistant output stage will not apply any current to the load.

[0022] When the steady state no longer exists, the voltage Vin20 is much larger than the voltage Vout20, the pull signal Vg2 will approach ground, and therefore the NMOS transistor 218 will be turned off. The push signal Vg1 will approach ground, and therefore the PMOS transistor 216 will be turned on. The result is the main output voltage 204 pushes a main current to the load. The decayed push signal Vg3 is equal to the push signal Vg1 plus the absolute

value of the voltage difference between the gate and the source of the PMOS transistor 304. Likewise, the decayed pull signal Vg4 is equal to the pull signal Vg2 minus the absolute value of the voltage difference between the gate and the source of the NMOS transistor 306. Since the NMOS transistor 218 is turned off, the NMOS transistor 214 will also be turned off. The PMOS transistor 216 is turned on, the decayed push signal Vg3 is able to turn on the PMOS transistor 212 to push an external current to the load. The final result is the assistant output stage will push an assistant current to the load. When the voltage Vin20 turns into a little larger than the voltage Vout20, the push signal Vg1 and the pull signal Vg2 will return to quiescent bias condition. Since Vg1 and Vg2 is decayed by PMOS transistor 304 and NMOS transistor 306, Vg3 and Vg4 will be not enough to turn on the PMOS transistor 212 and the NMOS transistor 214. Therefore the assistant output stage will not apply any current to the load. The load will be drove by the current from the main output stage 204 till the voltage Vin20 equals to the Vout20.

[0023] When the steady state no longer exists, the voltage Vin20 is much smaller than the voltage Vout20, the push signal Vg1 will approach Vdd, and therefore the PMOS transistor

216 will be turned off. The pull signal Vg2 will approach to Vdd, and therefore the NMOS transistor 218 will be turned on. The result is the main output voltage 204 will pull a main current from the load. Since the PMOS transistor 216 is turned off, the PMOS transistor 212 will also be turned off. The NMOS transistor 218 is turned on, the decayed pull signal Vg4 is able to turn on the NMOS transistor 214 to pull an external current from the load. The final result is the assistant output stage will pull an assistant current from the load. When the voltage Vin20 turns into a little smaller than the voltage Vout20, the push signal Vg1 and the pull signal Vg2 will return to quiescent bias condition. Since Vg1 and Vg2 are decayed by PMOS transistor 304 and NMOS transistor 306, Vg3 and Vg4 will be not enough for the PMOS transistor 212 and the NMOS transistor 214. Therefore, the assistant output stage will not pull any current from the load. The load will be drove by the current from the main output stage 204 till the voltage Vin20 equals to the Vout20.

[0024] The assistant output stage is an apparatus, which could provide extra current to the load. The assistant output stage is controlled by PMOS transistor 304 and NMOS transistor 306, which operate as a source follower. Thus,

the assistant output stage will be turned on after the main output stage is turned on, and be turned off before the main output stage is turned off. The assistant output stage is turned on/off automatically, and furthermore the assistant output stage does not consume static operating current. The problem of prior art, such as: offset voltage, pole/zero location, and linearity, will no longer exist. The slew rate of operational amplifier is increased without consume extra operating current and degrade stability.

[0025] Fig. 4 is the graph of the final push current and the final pull current at the node N25 versus the push and pull signal of OPAMP with and without this art. The final push current and the final pull current are obviously increased by the assistant output stage. In FIG.4, the push current with this art is larger than the push current without this art under the same push signal V01. Likewise, the pull current with this art is larger than the pull current without this art under the same pull signal V02. Therefore, the final push current or pull current is higher for the original OPAMP with this art. With the dynamic output stage in this art, it is easy to enhance the slew rate without increasing static operating current for the original OPAMP.

[0026] Accordingly, the circuit and method provided in the

present invention can be used to any circuit having at least two inputs, for example, a first input and a second input and a main current. The method of the invention includes that, first of all, detecting a first input and a second input. Secondly, generating a push current when a voltage of the second input is larger than a voltage of the first input and is enough to turn on at least one of the switches. Otherwise, generating a pull current when a voltage of the first input is larger than a voltage of the second input and is enough to turn on at least one of the switches. Thus, the push circuit and the pull circuit can be used to enlarge the main current to enhancement the slew rate. Moreover, the push current and the pull current further feed back to one of the first input and the second input. Furthermore, the push current and the pull current is turned on automatically after the main current is turned on, and is turned off automatically before the main current is turned off.

[0027] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and

variations of this invention provided they fall within the scope of the following claims and their equivalents.